REMARKS

Claim 1 has been amended to stress that the bonding pads on the upper chip are arranged in a line running perpendicular to the bonding pads on the substrate. Support is found in FIG. 3 of the drawings, and on page 6, lines 2-10 of the original specification. As noted therein, this arrangement makes it possible to reduce the size of the package in the horizontal direction. Neither the newly cited patent to Carson et al., employed to reject claim 1 under 35 USC §102(b) nor the Warren and Bruce et al. references, employed in combination to reject claims 1-8 under 35 USC §103(a) teach or suggest this construction, or the advantages resulting therefrom. Accordingly, it is submitted none of the art alone or in combination reasonably could be said to anticipate or render obvious the claimed invention.

The foregoing amendment clarifies the claims but it is not believed to raise any new issues which would require further search by the Examiner. Accordingly, entry of the foregoing amendment, and allowance of the Application are respectfully requested.

In the event there are any fee deficiencies or additional fees payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,

Norman P. Soloway
Attorney for Applicant
Reg. No. 24,315

CERTIFICATE OF FACSIMILE TRANSMISSION PURSUANT TO 37 CFR 1.6(d)

I hereby certify that this correspondence is being transmitted via facsimile to the United States Patent and Trademark Office, Attn. Examiner Chu at number 703-308-7722 on February 28, 2002.

By Sharon McKniff

HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C.
175 CANAL STREET
MANCHESTER, NH
03101-2335 U.S.A.

603-668-1400

MARKED COPY OF AMENDED CLAIM

SERIAL NO. 09/593,891

DOCKET: NEC DP-624

MARKED COPY OF AMENDED CLAIM:

1. (Twice Amended) A stacked semiconductor storage device comprising, in combination, a lower chip and an upper chip superimposed on a substrate, said semiconductor storage device further comprising:

a wiring substrate having wiring patterns thereon, interposed between said lower chip and said upper chip, for relaying electric connection between bonding pads on said upper chip and bonding pads on said substrate[.], wherein the bonding pads on said upper chip are arranged in a line running perpendicular to a line of bonding pads on the substrate.